DC and Transient Responses (i.e. delay) (some comments on power too!)

Michael Niemier

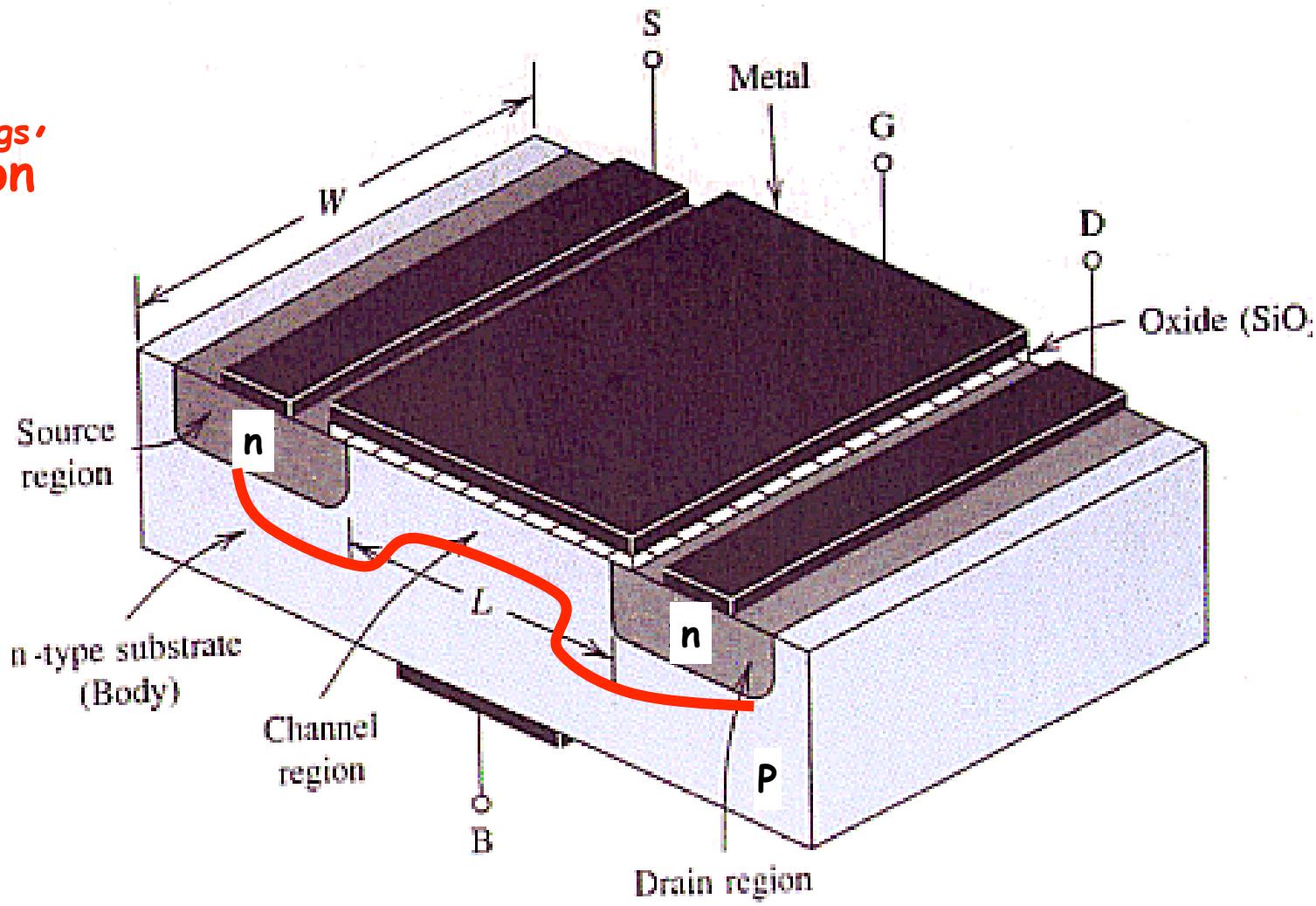
(Some slides based on lecture notes by David Harris)

Outline

- Today…
  - 1st…
    - Quickly review material from last time
  - 2nd…
    - Briefly think about transistor operation in context of logic gates
  - 3rd…
    - Use basic logic gates to study trends relating to power & delay in context of device scaling

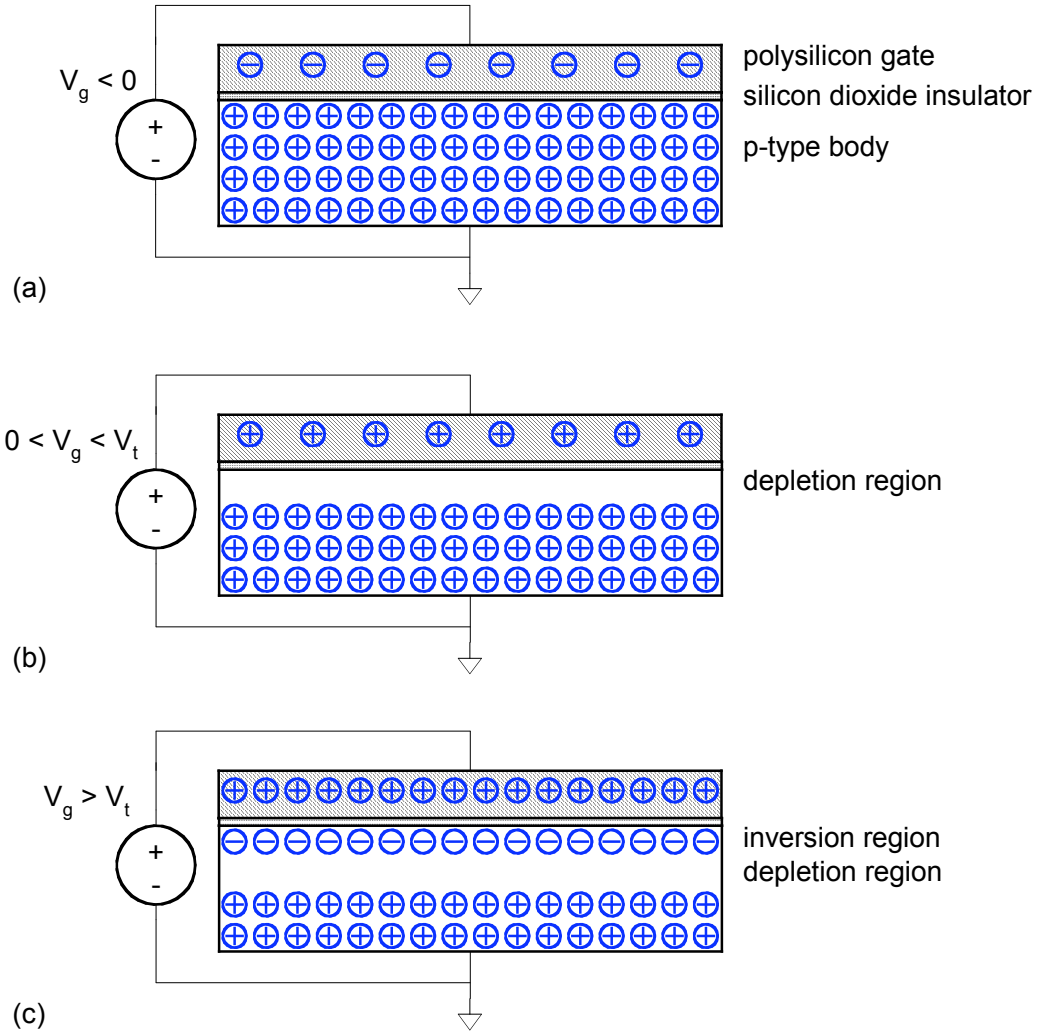
MOSFET cross section…

With applied V_{gs}, depletion region forms



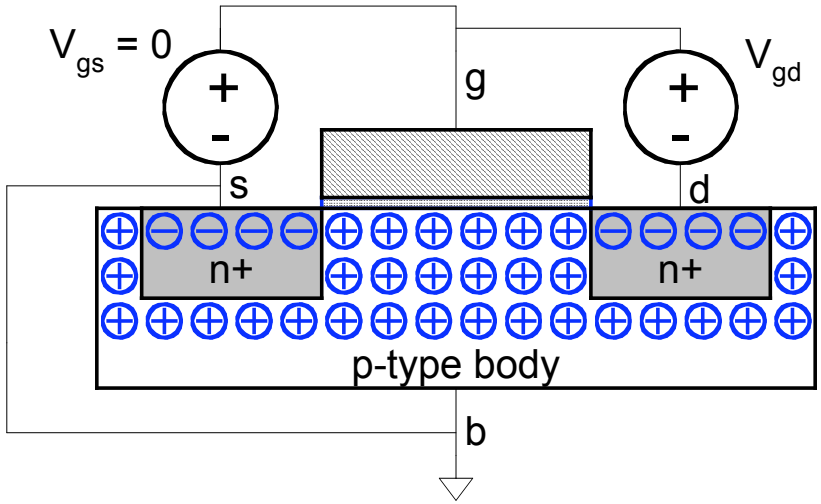
Review: MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes



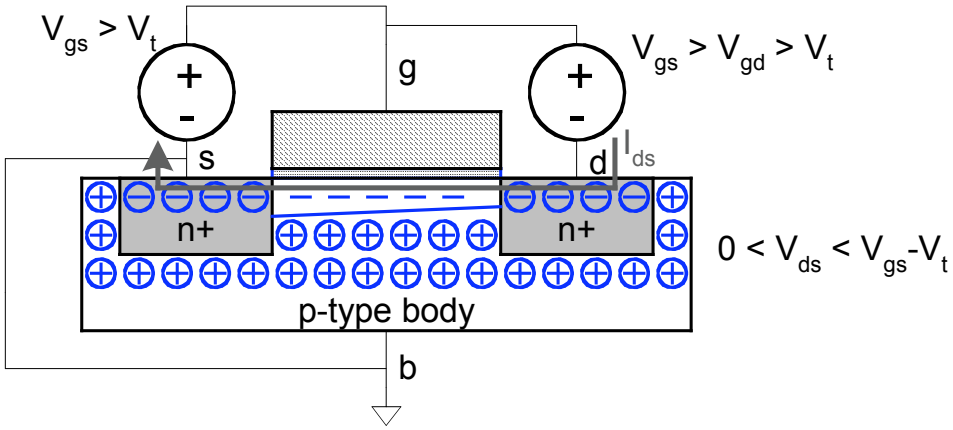
Review: nMOS Cutoff

- No channel formed, so no current flows
- $I_{ds} = 0$



Review: nMOS Linear

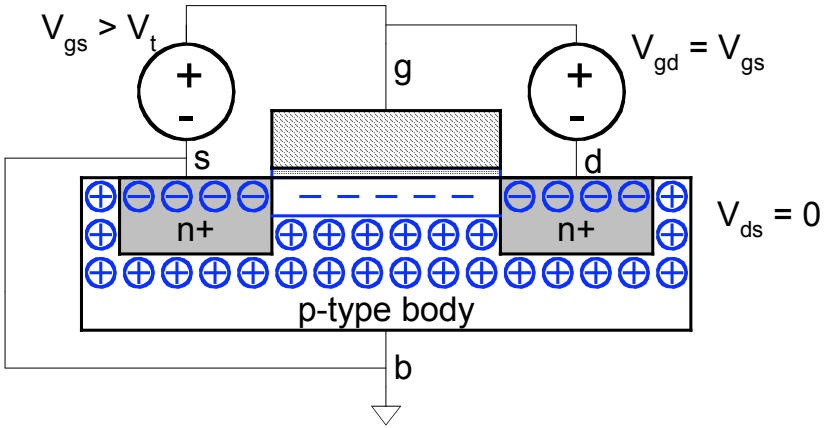
- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



$V_{gs} > V_t$

$V_{ds} > 0$, but $< (V_{gs} - V_t)$

(current flows)

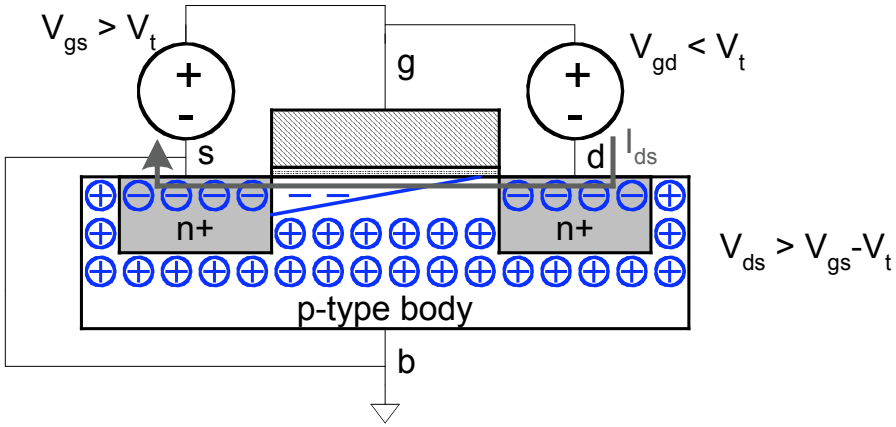


$V_{gs} > V_t$

$V_{ds} = 0$, no current

Review: nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source



$$V_{ds} > V_{gs} - V_t$$

Essentially, voltage difference over induced channel fixed at $V_{gs} - V$

(current flows, but saturates)

(or i_{ds} no longer a function of V_{ds})

nMOS I-V Summary

- ***Shockley* 1st order transistor models**

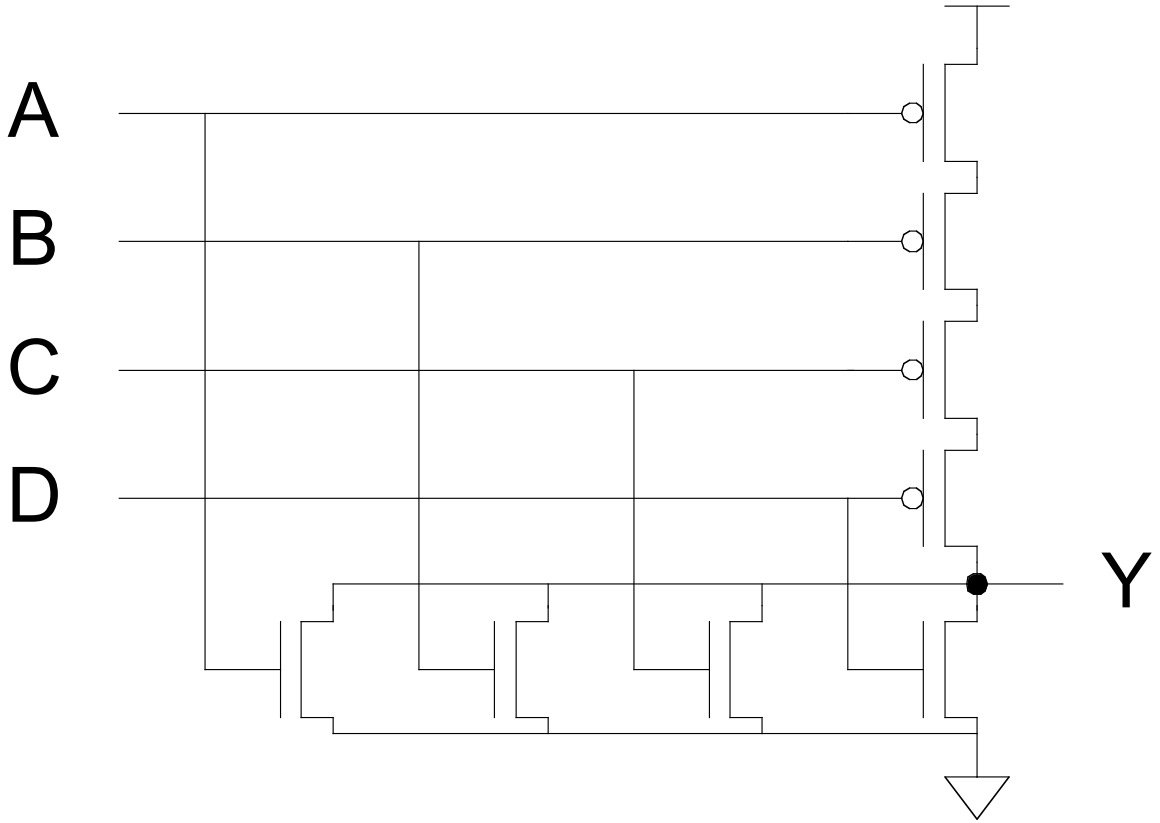
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

We'll start by considering logic gates in the context of transistor currents…

(for CMOS-based circuits…)

CMOS Gate Design

- 4-input CMOS NOR gate



A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

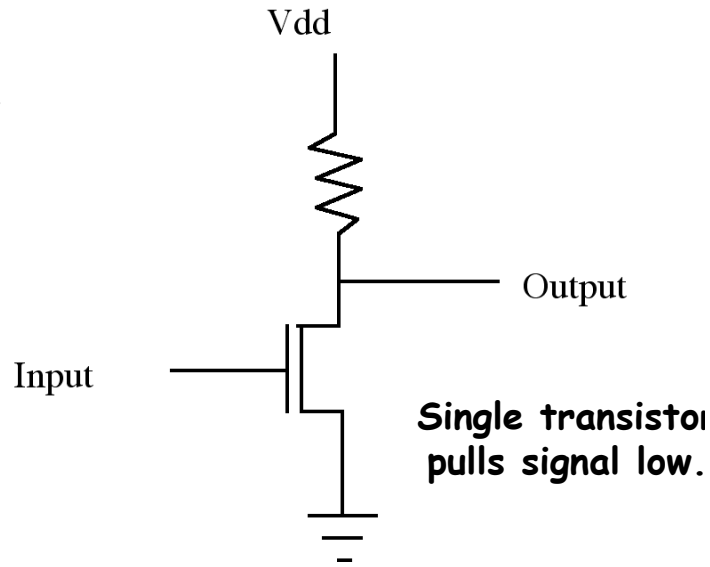
(2-input NOR for reference)

Why CMOS?

- High noise margins:
  - Voltage swing ~ = supply voltage
- No direct path between supply and ground rails under steady-state operating conditions
  - (I.e. when input and outputs remain constant)
  - Absence of current flow = no static power
    - But this isn't exactly true as we'll see…

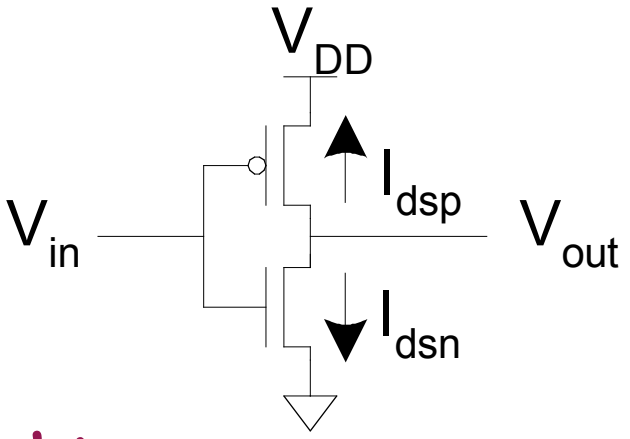
- All early Intel microprocessors NMOS only
  - (see NMOS inverter at right)

- Hard to achieve 0 static power
  - Put firm upper bound on # of gates
  - Necessitated move to CMOS in 1980s



1st, DC Response

- DC Response: V_{out} vs. V_{in} for a gate
- Ex: Inverter
  - When V_{in} = 0 --> V_{out} = V_{DD}
  - When V_{in} = V_{DD} --> V_{out} = 0
  - In between, V_{out} depends on transistor size and current
  - Want: $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - But graphical solution gives more insight



Transistor Operation

- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

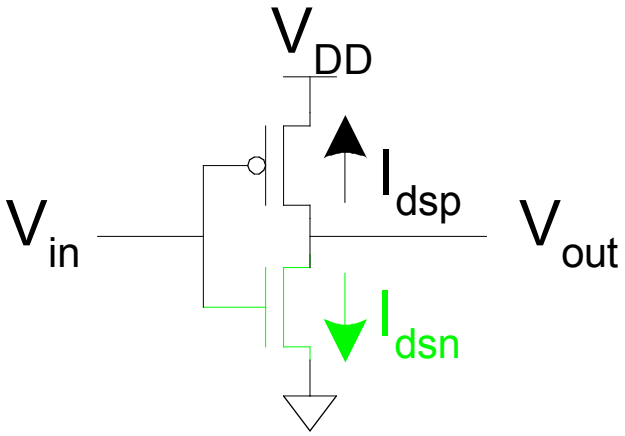
nMOS Operation

Recall…

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ Same	$V_{gsn} > V_{tn}$
	$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$

No Current | $V_{ds} < V_{gs} - V_t$ | $V_{ds} < V_{gs} - V_t$

In inverter context, what is V_{gs}, V_{ds} for NMOS device?

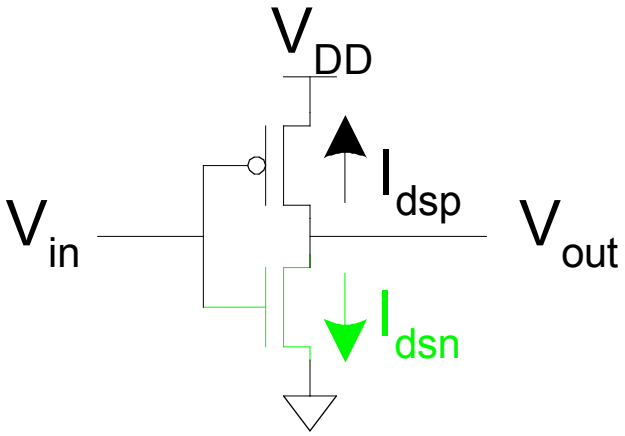


nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$

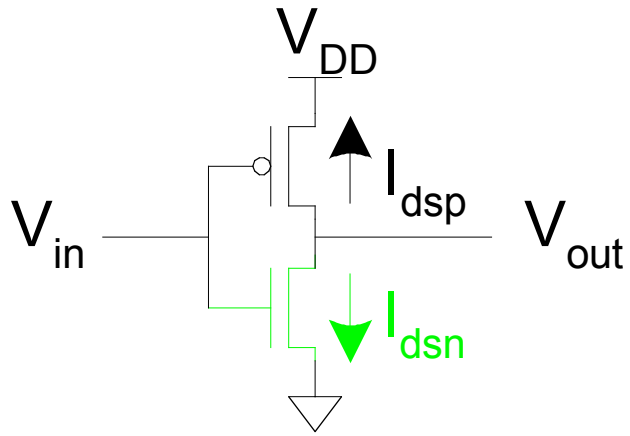


nMOS Operation (in context of inverter input V)

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$



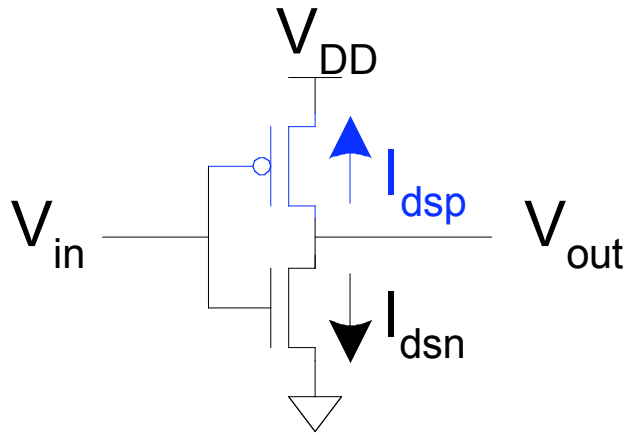
pMOS Operation
(for reference)

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$

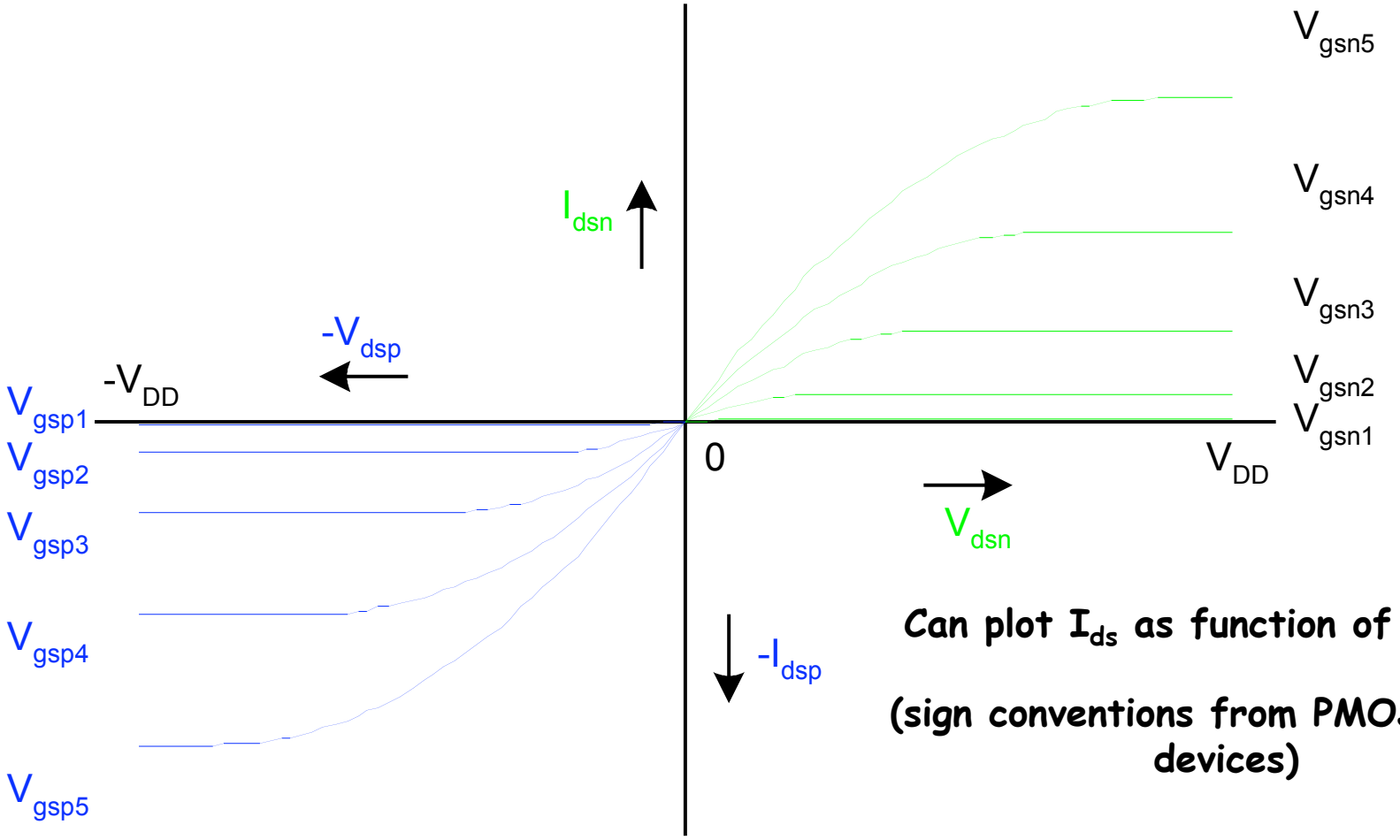
$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$



I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$



Can plot I_{ds} as function of V_{gs}, V_{dd}

(sign conventions from PMOS/NMOS devices)

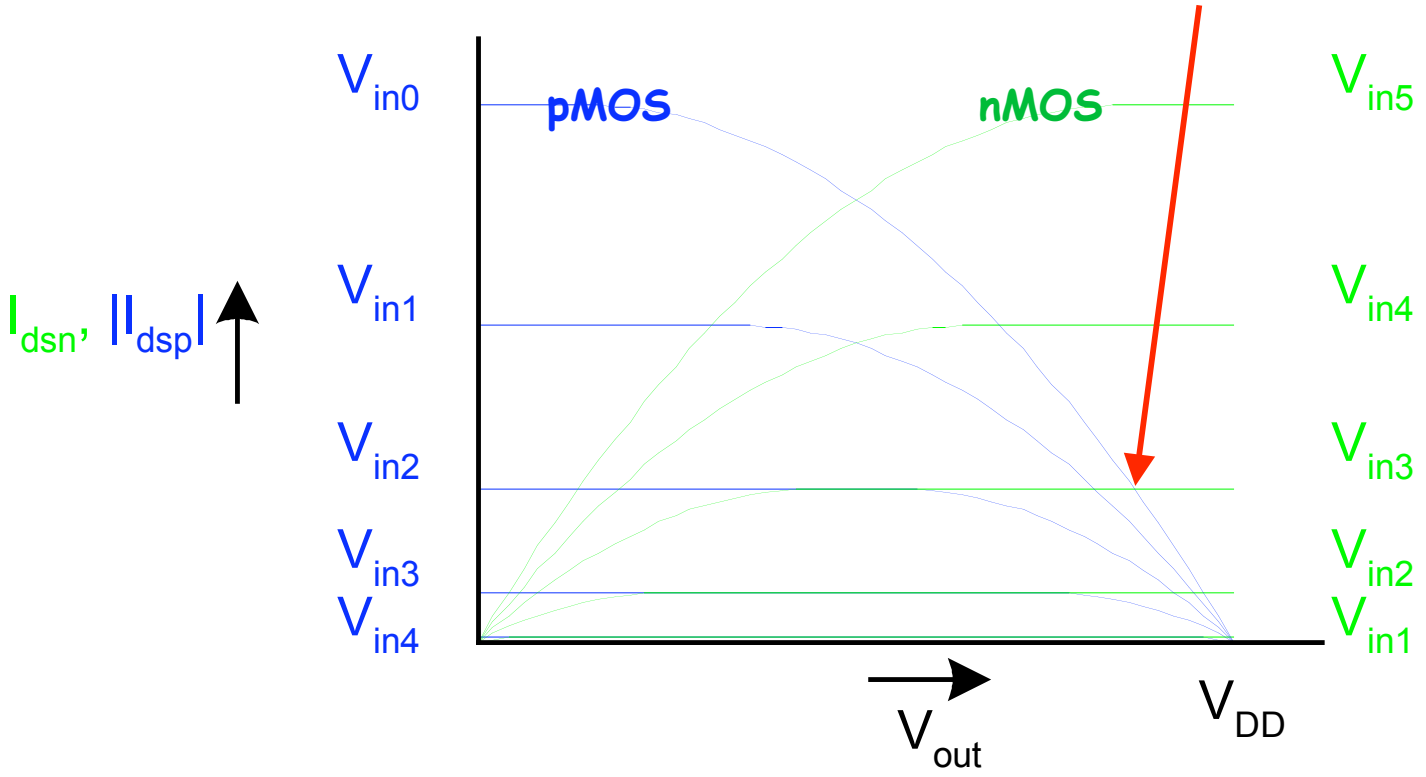
Load Line Analysis

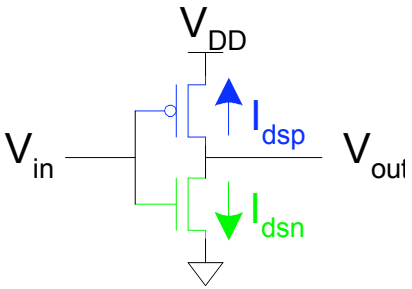
- For a given V_{in}:
  - Plot I_{dsn}, I_{dsp} vs. V_{out}
  - V_{out} must be where |currents| are equal in

(Translate lines onto same set of axes…)

(For DC operating point to be valid - consider graphical intersection of load lines…

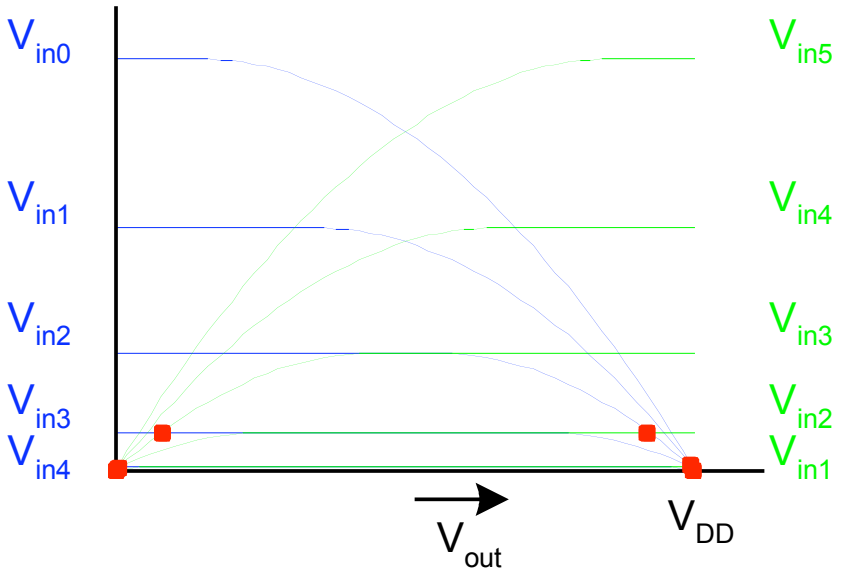
i.e. current in pMOS > current in nMOS

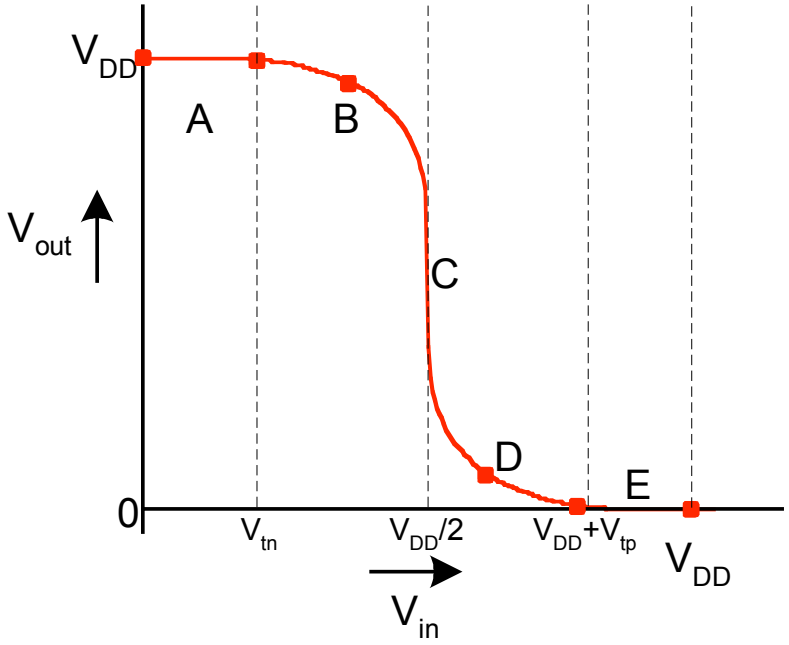




DC Transfer Curve

- Transcribe points onto V_{in} vs. V_{out} plot





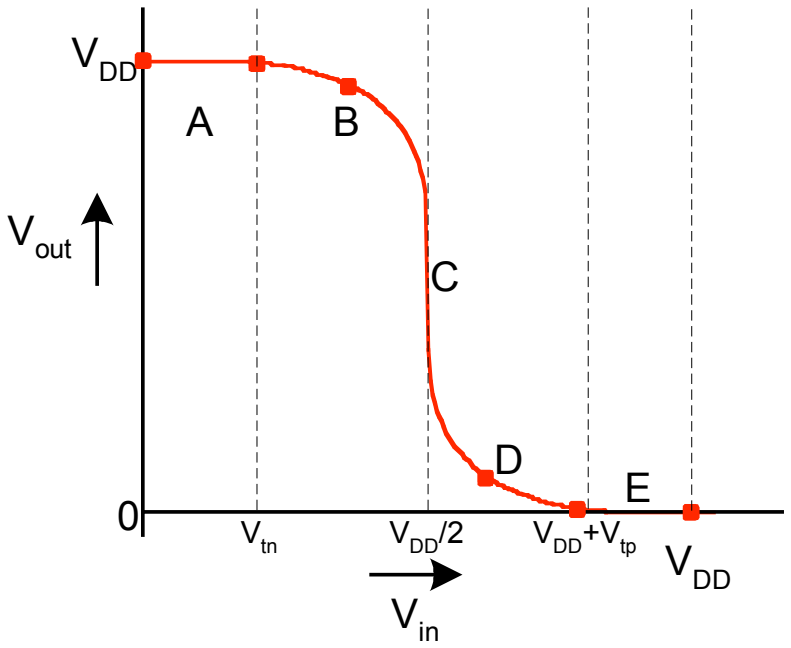
Comments:

- All operating points are located near high or low output levels
- The VTC of the inverter exhibits a very narrow transition zone
- This results from high gain during the switching transient
  - (When both NMOS, PMOS are in saturation and on simultaneously)
  - (In this region, small change in the input voltage results in a large output variation)

Operating Regions

- Revisit transistor operating regions

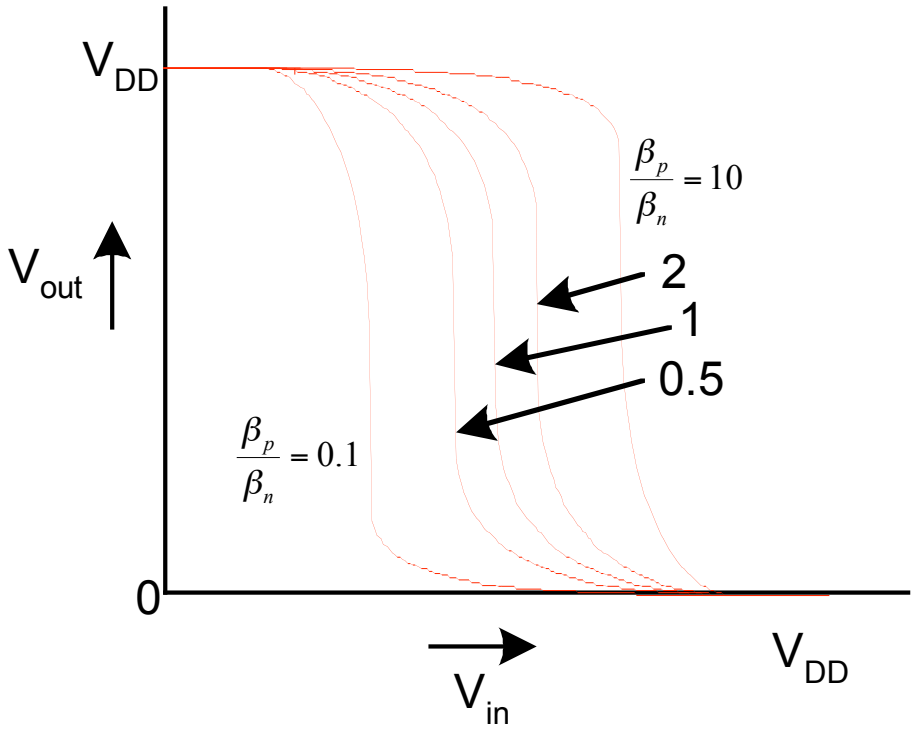
Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



A few more interesting points…

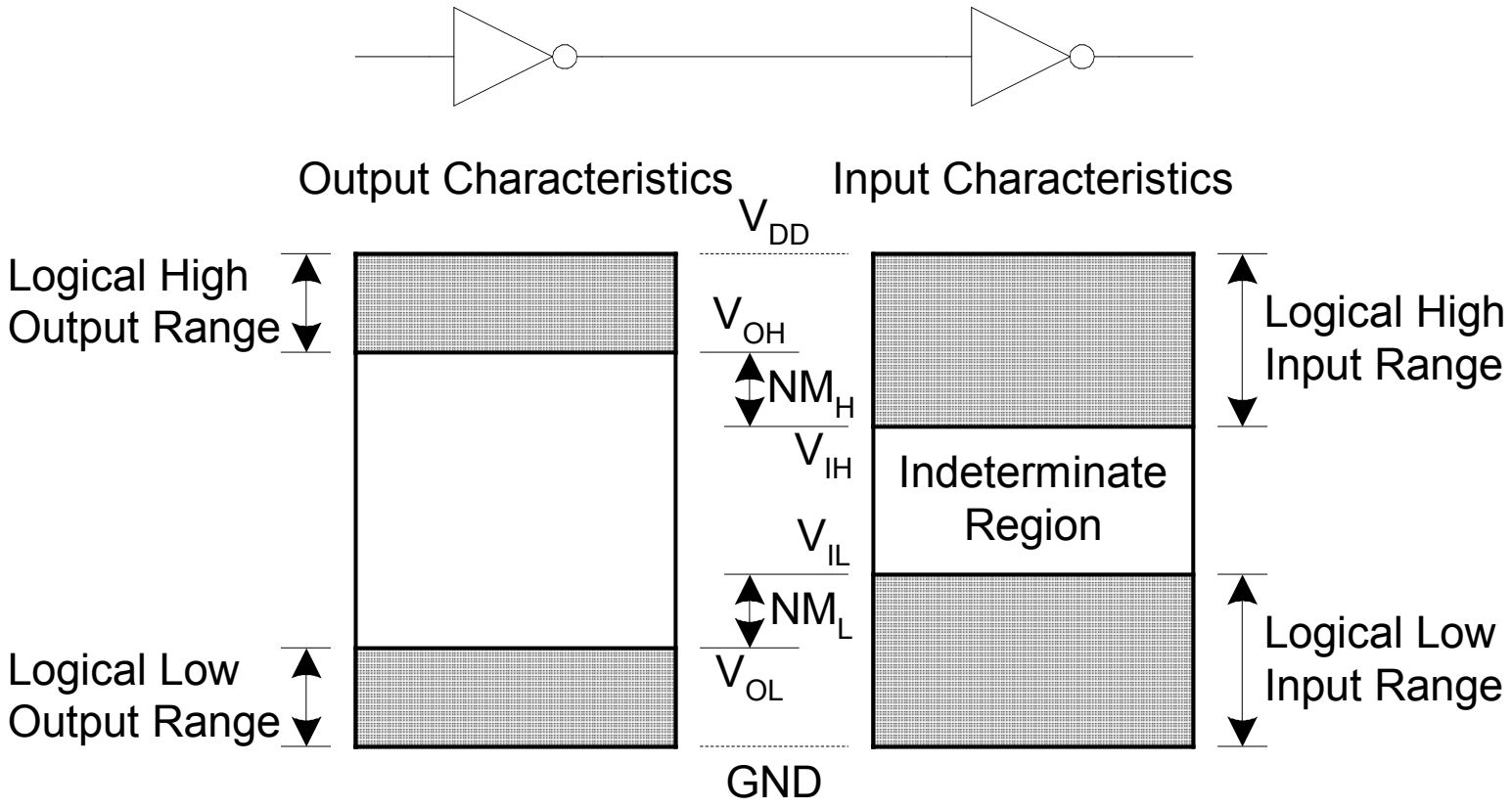
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



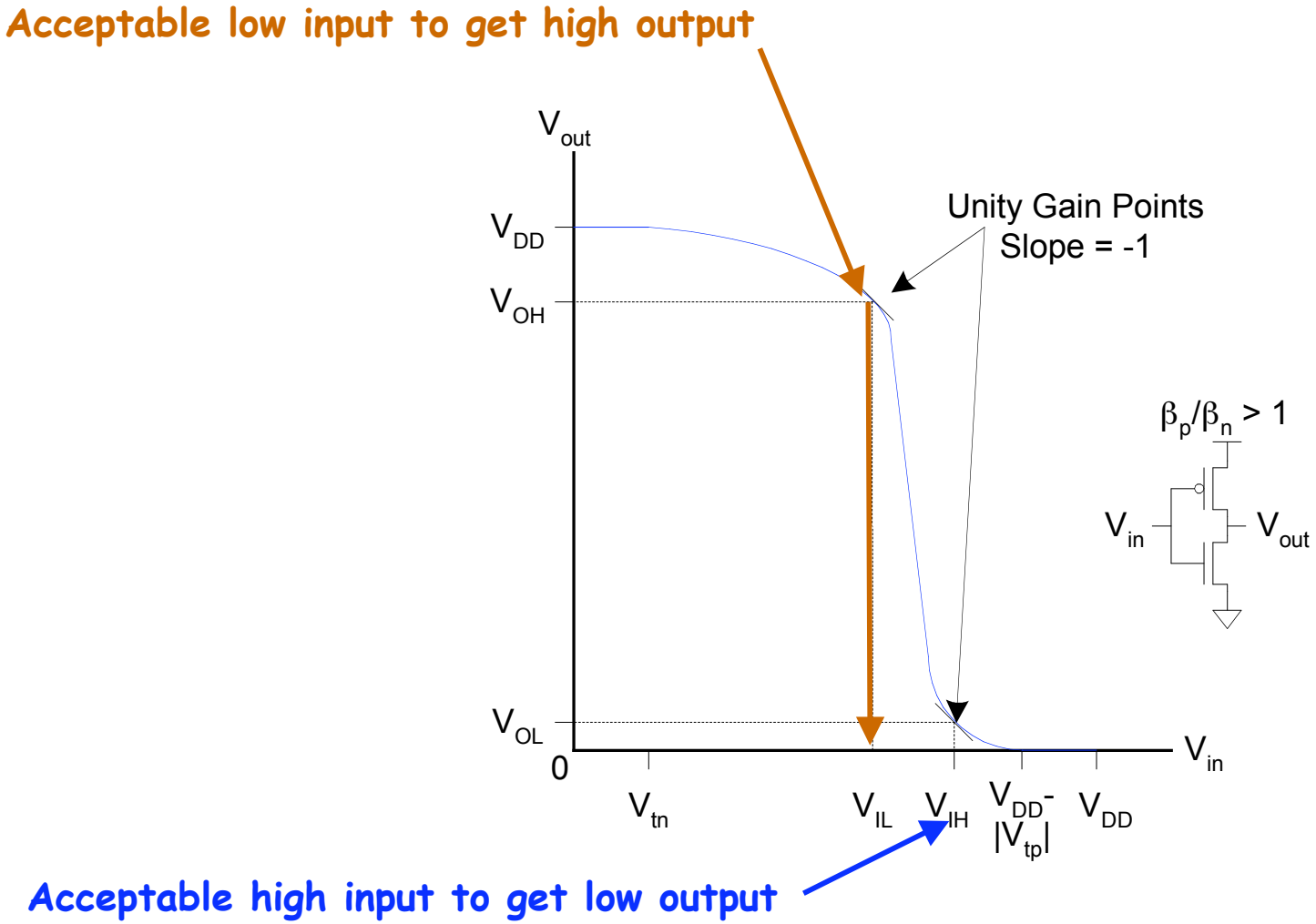
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



Supply voltage scaling

- As supply voltage scales down - which can be good as we'll see - can have problems
  - To a point (~0.5V), scaling Vdd improves gain
  - Beyond, DC characteristics become increasingly sensitive to variations in the device parameteres
    - E.g. transistor threshold
  - Scaling supply voltages reduces signal swing
    - Makes design more sensitive to external noise sources that don't scale.

Next, board discussion on transient response, power.